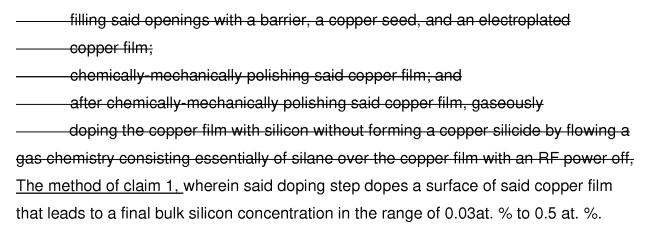
Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Listing of Claims:
1. (currently amended) A method for fabricating an integrated circuit, comprising the
steps of:
forming a dielectric layer;
forming openings in the dielectric layer;
filling said openings with a barrier, a copper seed, and an electroplated
copper film;
chemically-mechanically polishing said copper film; and
after chemically-mechanically polishing said copper film, forming a silicon nitride
layer by:
transferring the semiconductor body to a chamber;
gaseously doping the copper film with silicon without forming a copper
silicide by flowing a gas chemistry consisting of silane over the copper film <u>in the</u>
chamber with the RF power off prior to striking a plasma;
striking said plasma in said chamber after flowing said silane for at least
0.5 seconds; and
then flowing at least one nitrogen-containing source gas into said chamber
to deposit a silicon nitride layer over said copper interconnect.
2. (original) The method of claim 1, wherein said doping step dopes only a top region of
the copper film with silicon.
3. (currently amended)-A-method for fabricating an integrated circuit, comprising the
steps of:
forming a dielectric layer;
forming openings in the dielectric layer;

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- 4. (original) The method of claim 1, wherein said dielectric layer comprises an interlevel dielectric and an intrametal dielectric.
- 5. (original) The method of claim 4, wherein said openings comprise vias in the interlevel dielectric and trenches in the intrametal dielectric.
- 6. (original) The method of claim 1, wherein said doping step comprises flowing silane over the copper film for a duration in the range of 0.5 to 5 seconds at 325°C-425°C.
- 7. (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

providing a semiconductor body having a trench formed in a dielectric layer at a surface thereof;

forming a copper film over the semiconductor body including with said trench,

chemically-mechanically polishing the copper film to form a copper interconnect;

after said chemical-mechanical polish step, doping said copper interconnect with silicon without forming a silicide by flowing silane over a surface of the copper interconnect with an RF power off prior to striking a plasma;

wherein said doping step comprises part of a silicon nitride deposition process; and wherein said silicon nitride deposition process comprises the steps of:

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transferring the semiconductor body to a chamber;
performing said doping step by flowing silane in said chamber for a given
time prior striking said plasma in said chamber;
striking said plasma in said chamber after flowing said silane for at least
0.5 seconds; and
then flowing at least one nitrogen-containing source gas into said chamber
to deposit a silicon nitride layer over said copper interconnect.
8. (cancelled).
9. (previously presented) The method of claim 7, wherein said silane is flowed over the surface of the copper interconnect for a duration of approximately 3 seconds.

10. (previously presented) The method of claim 7, wherein said silane is flowed over the surface of the copper interconnect for a duration in the range of 0.05 to 5 seconds at 325°C to 425°C.

11-12. (cancelled)

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